REMARKS

Claims 2-9, 32-36, 64 and 65 are pending in the present application. Claims 1 and 10-16 have been cancelled from the application in this response, without prejudice to pursuing these claims in a divisional, continuation, continuation-in-part, or other application. Claims 2-9 and 32 have been amended, and new claims 64 and 65 have been added in this response. More specifically, claim 7 has been rewritten in independent form without narrowing the scope of this claim.

In the Final Office Action mailed February 27, 2004, claims 1-16 and 32-36 were rejected. More specifically, the status of the application in light of this Office Action is as follows:

(A) Claims 1-16 and 32-36 were rejected under 35 U.S.C. § 112, second paragraph;

(B) Claims 1, 2, 4-7 and 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,723,900 to Kojima et al. ("Kojima");

(C) Claims 10 and 15 were rejected under 35 U.S.C. § 102(b) as being anticipated by Japanese Patent No. 361114563 to Nishimura ("Nishimura");

(D) Claims 3, 7, 8, 10-14 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kojima in combination with U.S. Patent No. 6,544,814 to Yasunaga et al. ("Yasunaga");

(E) Claims 32-36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kojima and Yasunaga in combination with U.S. Patent No. 6,297,543 to Hong et al. ("Hong");

(F) Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishimura in combination with Japanese Patent No. 406177268 to Yoneda ("Yoneda");

(G) Claims 1-3, 5-9 and 32-34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,483,098 to Joiner ("Joiner") in combination with Yoneda; and

(H) Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Joiner, Yoneda, and Kojima.

A. Response to the Section 112 Rejection

Claims 1-16 and 32-36 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1 and 10-16 have been cancelled in this response and therefore the rejection of these claims is now moot. Claims 7 and 32 have been amended to delete the language the Examiner alleges is indefinite. Accordingly, the Section 112 rejection of claims 7 and 32 and their respective dependent claims should be withdrawn.

B. Response to the Section 102(b) Rejection of Claims 1, 2, 4-7 and 9

Claims 1, 2, 4-7 and 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by Kojima. Claim 1 has been cancelled in this response and therefore the rejection of this claim is now moot. As described below in detail, the rejection of claim 7 is improper because Kojima does not disclose or suggest all of the claim features.

1. Claim 7 is Directed to a Method of Packaging a Substrate Including Directing Laser Radiation Toward an Encapsulating Material on a Surface of the Substrate

Claim 7 is directed to a method for packaging a microelectronic substrate including disposing an encapsulating material in direct contact with a surface of the microelectronic substrate. The method further includes exposing a portion of the surface of the microelectronic substrate by removing a portion of the encapsulating material in direct contact with the surface of the microelectronic substrate. Removing a portion of the encapsulating material includes directing laser radiation toward the encapsulating material. The microelectronic substrate is in an operable condition after a portion of the encapsulating material is removed. An advantage of the method in accordance with claim 1 is that removing a portion of the encapsulating material allows heat to be more effectively and efficiently removed from the microelectronic substrate.

2. Kojima Discloses a Method for Forming a Thin Semiconductor Device Including Grinding the Mold Resin and Semiconductor Chip to Planarize the Rear Surface of the Device

Kojima discloses a method for forming a thin, molded semiconductor device in which the thickness of the device is defined by the thickness of the lead frame. First, a semiconductor chip 13 is coupled to an inner lead 16 of a lead frame 12 such that the chip 13 projects above the lead frame 12 (Kojima, Figure 4G). Next, the semiconductor

chip 13 and the inner lead 16 are encapsulated with a resin 14 (Kojima, Figure 4H). "In this state, the semiconductor chip 13 and the mold resin 14 project out from the surface of the outer lead 15A." (Kojima, col. 4, ll. 59-61.) "After molding with the resin 14, a rear surface 13a of the semiconductor chip 13 is ground so as to be flush with the upper surface of the outer lead 15." (Kojima, col. 3, ll. 59-61; Figure 4I.) Accordingly, the semiconductor chip 13 is thinned to create a planar surface across the outer lead 15 and the rear surface 13a of the chip 13.

3. Kojima Fails to Disclose a Method of Packaging a Substrate Including Directing Laser Radiation Toward an Encapsulating Material on the Substrate

Kojima fails to disclose a method of packaging a microelectronic substrate including, *inter alia*, "removing a portion of the encapsulating material in direct contact with the surface of the microelectronic substrate" by "directing laser radiation toward the encapsulating material," as recited in claim 7. To the contrary, Kojima discloses grinding the mold resin 14 and rear surface 13a of the semiconductor chip 13 so that the mold resin 14 and rear surface 13a are flush with the upper surface of the outer lead 15. Consequently, Kojima fails to disclose each and every element of claim 7, and in fact expressly teaches away from the elements of claim 7, as described in detail below. Therefore, the Section 102(b) rejection of claim 7 should be withdrawn.

Claims 2, 4-6 and 9 have been amended to depend from claim 7. Accordingly, the Section 102(b) rejection of these claims should be withdrawn for the reasons discussed above with reference to claim 7 and for the additional features of these claims.

C. Response to the Section 102(b) Rejection of Claims 10 and 15

Claims 10 and 15 were rejected under 35 U.S.C. § 102(b) as being unpatentable over Nishimura. Claims 10 and 15 have been cancelled in this response and therefore the rejection of these claims is now moot.

D. Response to the Section 103(a) Rejection of Claims 3, 7, 8, 10-14 and 16

Claims 3, 7, 8, 10-14 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kojima in combination with Yasunaga. Claims 10-14 and 16 have been cancelled in this response and therefore the rejection of these claims is now moot. For the reasons described below, one skilled in the art would not be motivated to combine Kojima and Yasunaga to include the features of claim 7.

1. Yasunaga Discloses a Method of Manufacturing Packaged Semiconductor Devices

Yasunaga discloses a method of packaging semiconductor chips. First, the semiconductor chips are mounted to the surface of an insulating substrate and electrodes on the chips are electrically connected to conductive patterns on the substrate. Next, the chips are encapsulated with a transfer mold resin, and electrode balls are formed on the side of the substrate opposite the chips. After forming the balls, a laser cuts through the mold resin and the substrate to dice the semiconductor devices.

2. One Skilled in the Art Would Not Be Motivated to Modify Kojima's Method to Cut the Mold Resin and Semiconductor Chip With the Laser Disclosed in Yasunaga

One skilled in the art would not be motivated to modify Kojima's method to cut the mold resin and semiconductor chip with the laser disclosed in Yasunaga because such a modification has numerous disadvantages. First, if one were to modify Kojima's method as the Examiner suggests, the laser would have to cut both the mold resin and the back side of the semiconductor chip so that the surface of the mold resin and the "rear surface 13a of the semiconductor chip 13 [would be] [] flush with the upper surface of the outer lead 15." (Kojima, col. 3, ll. 59-61; Figure 4I.) It is difficult to precisely control the depth of a laser cut—and would be especially difficult to precisely control the depth while cutting two different materials, namely the chip and mold resin. This is unlike the method disclosed in Yasunaga, in which the laser dices semiconductor devices and controlling the depth of the cut is not an issue. Accordingly, it would be disadvantageous to modify Kojima's method to cut the mold resin and semiconductor chip with Yasunaga's laser because of the difficulty in controlling the depth of the cut

and creating a planar surface across the outer lead 15 and the rear surface 13a of the chip 13.

Second, cutting Kojima's semiconductor chip with Yasunaga's laser would generate significant heat in the chip that may cause dopants in the chip to diffuse. The diffusion of dopants in the chip can result in defective active devices and an inoperable chip. Third, the heat from the laser may break the bonds between the mold resin, semiconductor chip, and/or lead because each component has a different coefficient of thermal expansion. For example, the difference in the coefficients of thermal expansion may cause the bump 17 at the tip of the inner lead 16 to detach from the electrode pad 18 of the chip 13. If the bonds between any of the components were to break, the semiconductor chip may become defective or inoperable. Because the Examiner's proposed modification of Kojima's method would have numerous disadvantages, one skilled in the art would not be motivated to make such a modification. Accordingly, the Section 103(a) rejection of claim 7 should be withdrawn.

Claims 3 and 8 have been amended to depend from claim 7. Accordingly, the Section 103(a) rejection of these claims should be withdrawn for the reasons discussed above with reference to claim 7 and for the additional features of these claims.

E. Response to the Section 103(a) Rejection of Claims 32-36

Claims 32-36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kojima and Yasunaga in combination with Hong. Independent claim 32 includes, *inter alia*, features generally similar to those described above with reference to claim 7. Accordingly, claim 32 is patentable over Kojima and Yasunaga for the reasons discussed above with reference to claim 7 and for the additional features of claim 32. Furthermore, Hong fails to cure the above-noted deficiencies of Kojima and Yasunaga as references supporting a *prima facia* case of obviousness under Section 103(a). For example, Hong discloses a semiconductor chip and a plurality of leads mounted to the chip and electrically connected to the chip with corresponding metal wires. The semiconductor chip is partially encapsulated with a molding compound and has a heat sink attached to one surface. Accordingly, Hong provides no motivation to modify Kojima's method to include "directing a source of laser radiation toward the second

surface of the microelectronic substrate to remove at least a portion of the encapsulating material adjacent to the second surface and expose the second surface," as recited in claim 32. Therefore, the Section 103(a) rejection of claim 32 should be withdrawn.

Claims 33-36 depend from claim 32. Accordingly, the Section 103(a) rejection of these claims should be withdrawn for the reasons discussed above with reference to claim 32 and for the additional features of these claims.

F. Response to the Section 103(a) Rejection of Claim 13

Claim 13 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Nishimura and Yoneda. Claim 13 has been cancelled in this response and therefore the rejection of this claim is now moot.

G. Response to the Section 103(a) Rejection of Claims 1-3, 5-9 and 32-34

Claims 1-3, 5-9 and 32-34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Joiner and Yoneda. Claim 1 has been cancelled and therefore the rejection of this claim should be withdrawn. For the reasons described below, one skilled in the art would not be motivated to combine Kojima and Yasunaga to include the features of claim 7 or 32.

1. Joiner Discloses a Partially Encapsulated Semiconductor Die Having an Opening

Joiner discloses a semiconductor die 12 with an active surface 13 and an inactive surface 14. The active surface 13 and a portion of the inactive surface 14 are encapsulated. "As shown in FIG. 2, encapsulant 22 does not completely encapsulate inactive surface 14 of semiconductor die 12, but rather encompasses an opening 23 in the package body to expose a portion of the inactive surface 14, wherein opening 23 can be formed by adding a boss or a pedestal to the mold tool. This structure has several advantages. . . . [T]he die opening acts as a pressure venting path for moisture to exit the package during the vapor phase or solder reflow operation. Because the internal vapor pressure is able to be released through the opening in the package body,

the plastic semiconductor package of the present invention tends not to crack or popcorn." (Joiner, col. 3, l. 52 - col. 4, l. 9.)

2. Yoneda Discloses a Semiconductor Device Having an Encapsulated Die and a Heat Sink with an Exposed Surface

Yoneda discloses a method of encapsulating a semiconductor device. First, a semiconductor chip 11 is attached to a first surface of a heat sink 12. Next, the chip 11 and the heat sink 12 are placed into a mold and encapsulated. After encapsulation, a laser removes a portion of the encapsulant from a second surface of the heat sink 12 which is opposite the first surface. As such, the semiconductor chip 11 is encapsulated, and the heat sink 12 has an exposed surface.

3. Joiner and Yoneda Fail to Disclose or Suggest a Method of Packaging a Substrate Including Disposing an Encapsulating Material in Direct Contact with the Substrate and Exposing a Portion of a Surface of the Substrate by Removing a Portion of the Encapsulating Material

Joiner and Yoneda fail to disclose a method of packaging a microelectronic substrate including, *inter alia*, "disposing an encapsulating material in direct contact with a surface of the microelectronic substrate; and exposing at least a portion of the surface of the microelectronic substrate by removing a portion of the encapsulating material in direct contact with the surface of the microelectronic substrate," as recited in claim 7. For example, although Joiner discloses disposing an encapsulant in direct contact with a surface of the semiconductor die 12, Joiner does not disclose removing a portion of the encapsulant in direct contact with the semiconductor die 12. To the contrary, Joiner discloses adding a boss or pedestal to the mold tool to form the opening 23 in the encapsulant 22 during the molding process. Yoneda also discloses disposing an encapsulating material in direct contact with a surface of a semiconductor chip 11, but does not disclose removing a portion of the encapsulating material in direct contact with the semiconductor chip 11. Rather, Yoneda discloses removing a portion of the encapsulant from a surface of the heat sink 12. Accordingly, the combination of Joiner and Yoneda fails to disclose each and every feature of claim 7.

Moreover, one of ordinary skill in the art would not be motivated to modify Joiner or Yoneda to include the features of claim 7. For example, there is no motivation for, as the Examiner suggests, "removing a portion of the encapsulating material in direct contact with the surface of the microelectronic substrate of Joiner . . . in order to provide a[n] . . . exposed surface structure to attach [the] heat sink." (Final Office Action, p. 9, ll. 13-17.) If the Examiner is suggesting removing a portion of the encapsulant 22 adjacent to the active surface 13 of the die 12 in Joiner's device, one of ordinary skill in the art would not be motivated to remove the encapsulant protecting the active side of the die, thereby exposing the active side and internal components of the die to potential contamination and damage. If the Examiner is suggesting removing a portion of the encapsulant proximate to the inactive surface 14 of the die 12, the Examiner must also be suggesting placing encapsulant in the opening 23 and then removing that encapsulant from the opening 23, because Joiner does not disclose placing encapsulant in the opening 23. Joiner, however, specifically teaches away from placing encapsulant 22 in the opening 23 because the "opening acts as a pressure venting path for moisture to exit the package during the vapor phase or solder reflow operation. Because the internal vapor pressure is able to be released through the opening in the package body, the plastic semiconductor package of the present invention tends not to crack or popcorn." (Joiner, col. 4, ll. 4-9.) Accordingly, one of ordinary skill in the art would not be motivated to modify Joiner's device to place encapsulant in the opening. Consequently, the Section 103(a) rejection of claim 7 should be withdrawn because (a) the applied references fail to disclose each and every element of claim 7, and (b) there is no motivation or suggestion to modify the references to include the elements of claim 7.

Claims 2, 3, 5, 6, 8 and 9 have been amended to depend from claim 7. Accordingly, the Section 103(a) rejection of these claims should be withdrawn for the reasons discussed above with reference to claim 7 and for the additional features of these claims.

Independent claim 32 includes, *inter alia*, features generally similar to those described above with reference to claim 7. Accordingly, the Section 103(a) rejection of

claim 32 should be withdrawn for the reasons discussed above with reference to claim 7 and for the additional features of claim 32.

Claims 33 and 34 depend from claim 32. Accordingly, the Section 103(a) rejection of claims 33 and 34 should be withdrawn for the reasons discussed above with reference to claim 32 and for the additional features of these claims.

H. Response to the Section 103(a) Rejection of Claim 4

Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Joiner, Yoneda, and Kojima. Claim 4 depends from claim 7 and, accordingly, is patentable over Joiner and Yoneda for the reasons discussed above with reference to claim 7 and for the additional features of claim 4. Furthermore, Kojima fails to cure the above-noted deficiencies of Joiner and Yoneda as references supporting a *prima facia* case of obviousness under Section 103(a). For example, Kojima does not provide motivation to place encapsulant in the opening of Joiner's device. Therefore, the Section 103(a) rejection of claim 4 should be withdrawn.

I. New Claims 64 and 65 Are Patentable Over the Cited References

New claim 64 includes, *inter alia*, features generally similar to claim 32. Accordingly, claim 64 is patentable over the cited references for the reasons discussed above with reference to claim 32 and for the additional features of claim 64. For example, claim 64 recites, *inter alia*, "mounting the microelectronic substrate to a dielectric support member with a first surface of the microelectronic substrate facing the dielectric support member and a second surface of the microelectronic substrate facing opposite the first surface." Kojima's chip 13 is attached to an inner lead 16 and an outer lead 15 both of which are not dielectric.

New claim 65 includes, *inter alia*, features generally similar to claim 32. Accordingly, claim 65 is patentable over the cited references for the reasons discussed above with reference to claim 32 and for the additional features of claim 65. For example, claim 65 recites, *inter alia*, "mounting the microelectronic substrate to a surface of a support member with a first surface of the microelectronic substrate facing the surface of the support member and a second surface of the microelectronic

substrate facing away from the support member" and "disposing an encapsulating material over the second surface of the microelectronic substrate and at least a portion of the support member such that a first portion of the encapsulating material projects from the surface of the support member." Assuming for the sake of argument that the chip 13, outer lead 15A, and bottom surface of the outer lead 15A of Kojima's device correspond at least in part to the microelectronic substrate, support member, surface of the support member, respectively, of claim 65, Kojima's chip does not face the bottom surface of the outer lead and "a first portion of the encapsulating material" does not project from the bottom surface of the outer lead.

J. Conclusion

In light of the foregoing amendments and remarks, all of the pending claims are in condition for allowance. Applicant, therefore, requests reconsideration of the application and an allowance of all pending claims. If the Examiner wishes to discuss the above-noted distinctions between the claims and the cited references or any other

distinctions, the Examiner is encouraged to contact David Dutcher by telephone. Additionally, if the Examiner notices any informalities in the claims, he is also encouraged to contact David Dutcher to expediently correct any such informalities.

Respectfully submitted,
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